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INTEGRATED CIRCUIT PACKAGING DESIGN AND METHOD

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INTEGRATED CIRCUIT PACKAGING DESIGN AND METHOD

BACKGROUND

Electronic devices are often subjected to extreme conditions during their manufacture and/or during the manufacture of systems that include the electronic devices. For example, integrated circuits, capacitors and resistors may be heated to extremely high temperatures within a reflow oven in order to solder the devices to a circuit board of an electronic device. As electronic device geometries and tolerances decrease, the susceptibility of devices to heat and other environmental conditions generally increases. Current manufacturing techniques utilize gold stud bump bonding and/or anisotropic conductive film in an attempt to subject electrical devices to more moderate manufacturing conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side elevation of an apparatus according to some embodiments.

FIG. 2 is a diagram of a process according to some embodiments.

FIG. 3 is a bottom view of an integrated circuit die according to some embodiments.

FIG. 4 is a side elevation of an apparatus according to some embodiments.

FIG. 5 is a bottom view of an integrated circuit die according to some embodiments.

FIG. 6 is a bottom view of an integrated circuit die according to some embodiments.

FIG. 7 is a top view of an integrated circuit package according to some embodiments.

FIG. 8 is a bottom view of an integrated circuit package according to some embodiments.

FIGS. 9a and 9b are views of an integrated circuit die according to some embodiments.

FIG. 10 is a side elevation of a system according to some embodiments.

DETAILED DESCRIPTION

FIG. 1 is a side elevation of apparatus 1 according to some embodiments. Apparatus 1 includes integrated circuit (IC) die 10, interconnect elements 20, and IC package 30. FIG. 1 also illustrates beam 40, optic fiber 42, and laser 44 that may be used to electrically couple IC die 10 to IC package 30 according to some embodiments.

IC die 10 includes integrated active and/or passive electrical devices and may be fabricated using any suitable substrate material and fabrication techniques. IC die 10 may embody a "flip-chip" arrangement and may provide one or more functions. In some embodiments, IC die 10 comprises a microprocessor chip having a silicon substrate. IC die 10 may also or alternatively comprise an element of a polymer memory or a liquid crystal display. IC die 10 includes conductive contacts (not shown) that may be electrically coupled to the devices that are integrated into IC die 10.

Interconnect elements 20 may comprise Controlled Collapse Chip Connect (C4) solder bumps according to some embodiments. Interconnect elements 20 according to some embodiments may include one or more of stud-bumped interconnects, diffusion-bonded interconnects, and other types of interconnects. Interconnect elements 20 are in contact with respective ones of the conductive contacts of IC die 10, and are also in contact with respective ones of the conductive contacts (not shown) of IC package 30. One or more of the aforementioned conductive contacts may be coated with a conductive material such as solder paste and/or conductive epoxy prior to receiving a respective one of interconnect elements 20. The conductive material itself may be considered a conductive contact with which the interconnect element 20 is in contact.

IC package 30 may comprise any ceramic, organic, and/or other suitable material. Conductive contacts of IC package 30 may be electrically coupled to vias within IC package 30 that are in turn coupled to external I/O interfaces of IC package 30. In particular, through-hole pins 50 may be electrically coupled to the conductive contacts of IC package

30 so as to transmit power and I/O signals between IC die 10 and external devices. For example, pins 50 may be used to mount package 30 to a socket on a motherboard or directly to a motherboard.

Beam 40 may be directed to one of interconnect elements 20 after placement of IC die 10 on IC package 30. Beam 40 is emitted from optic fiber 42, which in turn receives beam 40 from laser 44. Laser 44 may comprise a soft beam laser and/or any other type of laser. According to some embodiments, beam 40 directs energy to one of interconnect elements 20 in order to reflow the interconnect element 20 without exposing IC die 10 to potentially damaging temperatures.

FIG. 2 is a diagram of process 60 according to some embodiments. Process 60 may be executed by one or more devices, and all or a part of process 60 may be executed manually. Process 60 may be executed by an entity different from an entity that manufactures IC die 10 and/or IC package 30.

Initially, at 61, first energy is directed to a first interconnect element. The first interconnect element forms a first electrical connection based at least on the first energy. In some embodiments of 61, optic fiber 42 is positioned to direct beam 40 to only one interconnect element 20. Optic fiber 42 and laser 44 may be mounted in fixed positions on a device that moves both elements to place optic fiber 42 in the proper position. In some embodiments, optic fiber 42 may be moved independently of laser 44 due to its flexibility.

FIG. 1 illustrates some embodiments in which beam 40 is used to direct energy to one of interconnect elements 20 at 61. FIG. 3 is a view of IC die 10, beam 40 and a portion of optic fiber 42 from a different perspective. As shown, beam 40 is controlled to direct energy to only one of interconnect elements 20.

Next, at 62, second energy is directed to a second interconnect element. The second interconnect element forms a second electrical connection based at least on the second energy. The second electrical connection may electrically couple a conductive contact of IC die 10 to a conductive contact of IC package 30. The dashed outlines of beam 40A and optic fiber 42A illustrate directing second energy to a second interconnect element

according to some embodiments. In this regard, the second energy may be directed in a manner similar to that described above with respect to the first energy.

The application of energy to an interconnect element 20 may form an electrical connection between a conductive contact of IC die 10 that contacts the interconnect element 20 and a conductive contact of IC package 30 that also contacts the interconnect element 20. Although the energy is described herein as "forming" an electrical connection, in some embodiments an electrical connection exists between the conductive contacts via interconnect element 20 prior to application of the energy thereto. In some embodiments of process 60, the first energy and/or the second energy may be provided by any other suitable currently- or hereafter-known laser-based or non-laser-based system.

The energy applied during process 60 assists in causing interconnect element 20 to reflow according to some embodiments. A new electrical connection is therefore formed between the conductive contacts that are in contact with interconnect element 20 after interconnect element 20 has cooled. FIG. 4 shows a side elevation of system 1 after the energy of beam 40 has been directed to each illustrated interconnect element 20. Interconnect elements 20 have reflowed based at least on the energy and, according to the illustrated embodiment, a shape of interconnect elements 20 has changed. Reflowed interconnect elements 20 may provide a suitable electrical and physical connection between IC die 10 and package 30. Elements of IC die 10 and IC package 30 according to some embodiments will be now described in more detail.

FIG. 5 is a bottom view of IC die 10 showing conductive contacts 15. Conductive contacts 15 may comprise gold and/or nickel-plated copper contacts fabricated upon IC die 10. In this regard, conductive contacts 15 may be recessed under, flush with, or extending above the illustrated surface of IC die 10. Conductive contacts 15 may be electrically coupled to the active and/or passive devices that are integrated into IC die 10.

FIG. 6 illustrates interconnect elements 20 disposed on die 10 according to some embodiments. Interconnect elements 20 may comprise C4 solder bumps fabricated onto conductive contacts 15 of IC die 10 as illustrated in FIG. 5. One or more of interconnect

elements 20 may therefore be electrically coupled to the active and/or passive devices of IC die 10 through one or more conductive contacts 15. An IC die according to some embodiments might not comprise interconnect elements 20 of FIG. 6. Rather, in some embodiments, conductive contacts 15 of IC die 10 are coupled to interconnect elements located on IC package 30 when IC die 10 is mounted on IC package 30.

As mentioned above, overheating of sensitive areas of IC die 10 may be avoided in some embodiments by directing energy to individual ones of interconnect elements 20. Conductive contacts 15 of die 10 (and any interconnect elements 20 coupled thereto) may therefore be disposed so as to avoid undesirable heat transfer to areas of IC die 10. For example, conductive contacts 15 may be disposed proximate to a perimeter of IC die 10 under an assumption that most sensitive devices are located at interior locations of IC die 10.

Conductive die contacts 15 may also be disposed so as to facilitate the individual delivery of energy to associated interconnect elements 20. For example, conductive die contacts 15 (and interconnect elements 20) may be disposed only around a perimeter of die 10. Accordingly, optic fiber 42 may be moved relatively around the perimeter of IC die 10 to direct energy to each of interconnect elements 20 in turn.

FIG. 7 is a top view of IC package 30 according to some embodiments. IC package 30 comprises conductive contacts 32 for interfacing with interconnect elements 20 of IC die 10. Conductive contacts 32 may comprise any combination of conductive material, including gold and/or nickel-plated copper contacts. Conductive contacts 32 may therefore be electrically coupled to the devices integrated in IC die 10 through interconnect elements 20 and through conductive contacts 15 of IC die 10.

FIG. 8 is a bottom view of IC package 30 according to some embodiments. Pins 50 are shown disposed around a perimeter of IC package 30, although any configuration of pins 50 may be used in conjunction with some embodiments. IC package 30 may define recess 34 in which land-side capacitors 60 reside. Land-side capacitors 60 may be mounted in recess 60 to assist the functionality of IC die 10 and/or to reduce resonance between IC package 30 and a board on which IC package 30 is mounted.

According to some embodiments, package 30 is a surface-mountable substrate such as an Organic Land Grid Array substrate that may be mounted directly onto a motherboard or mounted on a pinned interposer which mates with a socket of a motherboard. Packaging systems other than those mentioned herein may be used in conjunction with some embodiments.

FIGS. 9a and 9b show two instances of IC die 10 according to some embodiments. In each case, circular conductive contacts 15 are disposed on IC die 10 in a manner that may facilitate the direction of energy to each interconnect that is coupled to each conductive die contact 15. Arrows 70 illustrate beam paths that could be used to direct laser or other types of energy to interconnect elements 20 that are in contact with conductive contacts 15.

FIG. 10 illustrates a system according to some embodiments. System 100 includes system 1 of FIG. 1, memory 110 and motherboard 120. System 100 may comprise components of a desktop computing platform. Memory 110 may comprise any type of memory for storing data, such as a Single Data Rate Random Access Memory, a Double Data Rate Random Access Memory, or a Programmable Read Only Memory.

Memory 110 and motherboard 120 may be electrically coupled to IC die 10 of system 1. More particularly, motherboard 110 may comprise a memory bus (not shown) coupled to pins 50 and to memory 110. In operation, motherboard 120 may route input/output and power signals to pins 50 for transmission to IC die 10.

The several embodiments described herein are solely for the purpose of illustration. In some embodiments, IC package 30 is coupled to an interposer using some of the above-described embodiments for coupling IC die 10 to package 30. Some embodiments may include any currently or hereafter-known versions of the elements described herein. Therefore, persons skilled in the art will recognize from this description that other embodiments may be practiced with various modifications and alterations.